What is claimed is:

1. A method of manufacturing a system-on-chip semiconductor device, including a CMOS logic circuit portion and a DRAM portion, comprising the steps of:

forming at least a first transistor on a substrate at said CMOS logic circuit portion;

forming at least a second transistor on said substrate at said DRAM portion;

forming an interlayer film on said substrate at said CMOS logic circuit portion and on said substrate at said DRAM portion, covering said at least a first transistor and said at least a second transistor;

forming a groove in said interlayer film by removing a portion of said interlayer film at said DRAM portion;

forming a first polysilicon film on an upper surface of said interlayer film at said CMOS logic circuit portion and at said DRAM portion, and a second polysilicon film on an inner wall of said groove at said DRAM portion,

forming a first HSG on a surface of said first polysilicon film and a second HSG on a surface of said second polysilicon film; and

removing said first HSG and said first polysilicon film.

2. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 1,

wherein said step of forming said at least a first transistor includes a step of forming a first gate insulating layer, and

wherein said step of forming said at least a second transistor includes a step of forming a second gate insulating layer,

wherein said first gate insulating layer is thinner that said second gate insulating layer.

3. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 2,

wherein said at least a second transistor comprises a peripheral circuit transistor and a switching transistor, and

wherein said peripheral circuit transistor and said switching transistor have similar structures.

4. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 3, wherein said step of forming an interlayer film comprises steps of:

forming a first interlayer film comprising a silicon oxide layer; and thereafter

forming a second interlayer film comprising a BPSG film.

5. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 4, further comprising steps of:

forming an opening in said first interlayer film over a diffusion region of said switching transistor; and

forming a capacitor electrode in said opening in said first interlayer film,

wherein said capacitor electrode is connected to said diffusion region of said switching transistor.

6. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 5, wherein said groove is formed in said second interlayer film, and said second polysilicon is connected to said capacitor electrode.

7. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 6, further comprising steps of:

forming a first photoresist layer on said first HSG and a second resist layer on said second HSG; and

removing said first photoresist layer to expose said first HSG.

8. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 7, further comprising steps of:

forming a capacitor film on said first HSG after said step of removing said first photoresist layer; and

forming a upper electrode on said capacitor film.

9. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 8, wherein said capacitor film comprises a Ta_2O_5 film; and

further comprising a step of forming a TiN film on said Ta_2O_5 before said step of forming said upper electrode.

10. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 2, wherein said step of forming said at least a first transistor further comprises steps of:

forming a first gate electrode comprising polysilicon; and

doping the polysilicon of the first gate electrode with boron,

wherein said at least a first transistor comprises a p-channel transistor having said first gate.

11. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 10, wherein said step of forming at least a first transistor further comprises steps of:

forming a second gate electrode comprising polysilicon;

doping the polysilicon of the second gate electrode with phosphorous;

wherein said at least a first transistor comprises a n-channel transistor having said second gate.

12. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 2, wherein said step of forming an interlayer film comprises a step of forming a BPSG film.

13. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 12, wherein said step of forming an interlayer film further comprises a step of forming a silicon oxide layer prior to forming said BPSG film, wherein said BPSG film is formed on said silicon oxide film.

14. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 2, wherein said DRAM portion comprises a memory cell portion and a

peripheral circuit portion, and a surface area of said memory cell portion is 10 to 25% of a sum of surface areas of said DRAM portion and said CMOS logic circuit portion.

15. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 14, wherein said surface area of said memory cell portion is 50 to 60% of the surface area of said DRAM portion.

16. A method of manufacturing a system-on-chip semiconductor device including a CMOS logic circuit portion and a DRAM portion, said DRAM portion comprising a cylinder type capacitor, the method comprising the steps of:

forming a first transistor on a substrate at said CMOS logic circuit portion;

forming a second transistor on said substrate at said DRAM portion;

forming an interlayer film on said substrate at said CMOS logic circuit portion and on said substrate at said DRAM portion, covering said first transistor and said second transistor;

forming a groove in said interlayer film by removing a portion of said interlayer film at said DRAM portion;

forming a polysilicon film on a said interlayer film at said CMOS logic circuit portion and at said DRAM portion, and on a inner wall of said groove at said DRAM portion,

forming a HSG on a surface of said polysilicon film; and

removing said HSG and said polysilicon film from an upper surface of said interlayer film, retaining at least a portion of said HSG in said groove and at least a portion said polysilicon in said groove.

17. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 16,

wherein said step of forming said at least a first transistor includes a step of forming a first gate insulating layer, and

wherein said step of forming said at least a second transistor includes a step of forming a second gate insulating layer,

wherein said first gate insulating layer is thinner that said second gate insulating layer.

18. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 17, wherein said step of forming said first transistor further comprises steps of:

forming a first gate electrode comprising polysilicon; and

doping the polysilicon of the first gate electrode with boron,

wherein said first transistor comprises a p-channel transistor having said first gate.

19. The method of manufacturing a system-on-chip semiconductor device as claimed in claim 17, wherein said step of forming an interlayer film comprises a step of forming a BPSG film.